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In accordance with the development of the technology of semiconductor devices, especially, the development of the technology of transistor elements, the thickness of the gate oxide film has been getting thinner. With the progress of the technology of semiconductor devices, the gate oxide film of the transistor element is getting thinner and thinner. In order to protect the gate oxide film from moisture and others, the countermeasures against moisture and others are getting important. The U.S. Pat. No. 6,806,372 and Japanese Patent Application Laid-Open Publication No. Hei11-354271 are known as the known prior arts concerning the countermeasures against the moisture and others. In the technology described in the patent or the publication, a moisture resistant semiconductor element is formed, and the moisture resistant semiconductor element is sealed with a sealing agent. In addition, in the technology described in the patent or the publication, a semiconductor element is formed on a semiconductor substrate, and a protective tape is adhered to a surface of the semiconductor element. The technology of forming a moisture resistant semiconductor element and a moisture resistant semiconductor element, and sealing them with a sealing agent will be described in the following. As shown in the diagram of FIG. 1, on a silicon substrate 1, a semiconductor element 2 including a transistor 2a, a resistor 2b, and a capacitor 2c is formed. First, a silicon nitride (SiN) film 3 as a moisture resistant film is formed on the silicon substrate 1. A silicon oxide (SiO₂) film 4 is formed on the silicon nitride (SiN) film 3, and a silicon nitride (SiN) film 5 is formed on the silicon oxide (SiO₂) film 4. Next, as shown in FIG. 2A, a gate oxide film 6 is formed on the silicon nitride (SiN) film 5. Next, as shown in FIG. 2B, a polysilicon film 7 serving as a gate electrode is formed on the gate oxide film 6. Next, as shown in FIG. 2C, by using the polysilicon film 7 as a mask, phosphorus (P) is

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